WHAT IS CLAIMED IS:

1. A leadframe for an integrated circuit package comprising:

an outer frame;

a die pad portion disposed within said outer frame; and

a plurality of lead portions extending substantially inward from said outer frame towards said die pad portion,

wherein at least one of said plurality of lead portions has a recess formed therein.

2. The leadframe according to claim 1, wherein said recess comprises a channel formed through said lead portions.

3. The leadframe according to claim 2, wherein an inner surface of said channel has a geometrically-shaped cross-section.

4. The leadframe according to claim 2, wherein said channel is formed form one side of said lead portion to the opposite side thereof.

5. The leadframe according to claim 2, wherein an inner surface of said channel has one of a substantially rectangular-shaped, U-shaped, and V-shaped cross section.

6. The leadframe according to claim 1, wherein said recess comprises a dimple-shaped impression.

7. The leadframe according to claim 6, wherein the inner surface of said dimple-shaped impression is rounded.

8. The leadframe according to claim 6, wherein the inner surface of said dimple-shaped impression is squared.

9. The leadframe according to claim 1, further comprising a plurality of tie bars connecting said die pad portion to said outer frame portion, wherein at least one of said tie bars has a recess formed therein.

10. The leadframe according to claim 9, wherein said recess comprises a channel formed through said tie bar.

11. The leadframe according to claim 10, wherein said channel is formed from one side of said tie bar to the opposite side thereof.

12. The leadframe according to claim 9, wherein said recess comprises a dimple-shaped impression.

13. An integrated circuit package comprising:

a die pad having a first face and a second face opposite to said first face;

a plurality of leads each having a first face and a second face opposite to said first face, wherein

said plurality of leads is disposed substantially around at least a portion of said die pad, and

said first face of at least one of said plurality of leads has a recess formed therein, said recess having inner walls;

an integrated circuit chip having a first face and a second face opposite to said first face wherein said second face is coupled to said first face of said die pad;

a plurality of wires each linking said integrated circuit chip to one of said plurality of leads; and

an encapsulant enclosing said integrated circuit chip, said plurality of wires, said first face of said die pad, and a portion of said first face of each of said plurality of leads, wherein said encapsulant forms a plurality of side walls, and at least one of said side walls intersects said first face of said at least one of said plurality of leads between the inner walls of said recess formed therein.

14. The integrated circuit package according to claim 13, wherein:

a majority of said plurality of leads has a recess formed therein, said recess having inner walls; and

said at least one of said plurality of side walls intersects said first face of said majority of said plurality of leads between the inner walls of said recess formed therein.

15. The integrated circuit package according to claim 13, wherein said recess comprises a channel formed through said lead.

16. The integrated circuit package according to claim 15, wherein said channel is formed from one side of the lead to the opposite side thereof.

17. The leadframe according to claim 13, wherein said recess comprises a dimple-shaped impression.

18. An integrated circuit package, comprising:

a die pad;

a plurality of leads, each having a first face and a second face opposite to the first face, wherein at least on of said plurality of leads has a recess formed in said first face thereof, said recess having at least two inner walls;

an IC chip coupled to said die pad;

a plurality of wires connecting said integrated circuit chip to said plurality of leads; and

an encapsulant enclosing said integrated circuit chip, said plurality of wires, said dies pad, and a portion of at least one of said plurality of leads, wherein said encapsulant forms a plurality of side walls, at least one of which intersects said at least one lead between said inner walls of said recess formed therein, and wherein said encapsulant fills said recess.

19. A method of assembling an integrated circuit package, comprising:

providing:

a die pad having a first face and a second face opposite to said first face,

a plurality of leads each having a first face and a second face opposite to said first face, wherein said first face of at least one of said plurality of leads has a recess formed therein, said recess having inner walls, and

an integrated circuit chip having a first face and a second face opposite to said first face;

coupling said second face of said integrated circuit chip to said first face of said die pad;

electrically connecting said integrated circuit chip to said plurality of leads;

enclosing said integrated circuit chip, said first face of said die pad, and a portion of said first face of each of said plurality of leads with an encapsulant, thereby forming a plurality of side walls, at least one of said side walls intersecting the first face of said at least one of said plurality of leads between the inner walls of said recess formed therein.

20. The method according to claim 19, wherein said recess comprises a channel formed through said lead.

21. The method according to claim 20, wherein said channel is formed from one side of said lead to the opposite side thereof.

22. The method according to claim 19, wherein said recess comprises a dimple-shaped impression.